Speculatively Granting Conflicting Accesses on Hardware Transactional Memory

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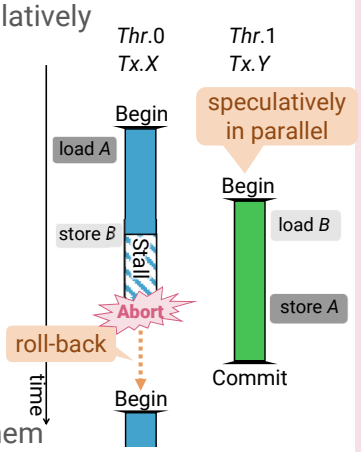
Hardware Transactional Memory (HTM)

- Transactions (Tx) are speculatively executed in parallel.
- HTM guarantees two properties for Tx.
  - ***Atomicity***
    - Each Tx must not be executed partially.
  - ***Isolation***
    - The result of concurrently executed Tx must be same as sequentially executed.
- Accesses that can violate them are detected as ***conflicting accesses***



Conflicting Accesses that can be Granted

- After the ***last-touch*** of a shared variable, accesses to the variable by other concurrent Tx will not violate *Isolation*.

```
BEGIN_TRANSACTION(0);
count++;

switch(op){
  case 0:  enqueue_right();      break;
  case 1:  dequeue_right();      break;
  case 2:  enqueue_left();       break;
  case 3:  dequeue_left();       break;
}
   :
COMMIT_TRANSACTION(0);
```

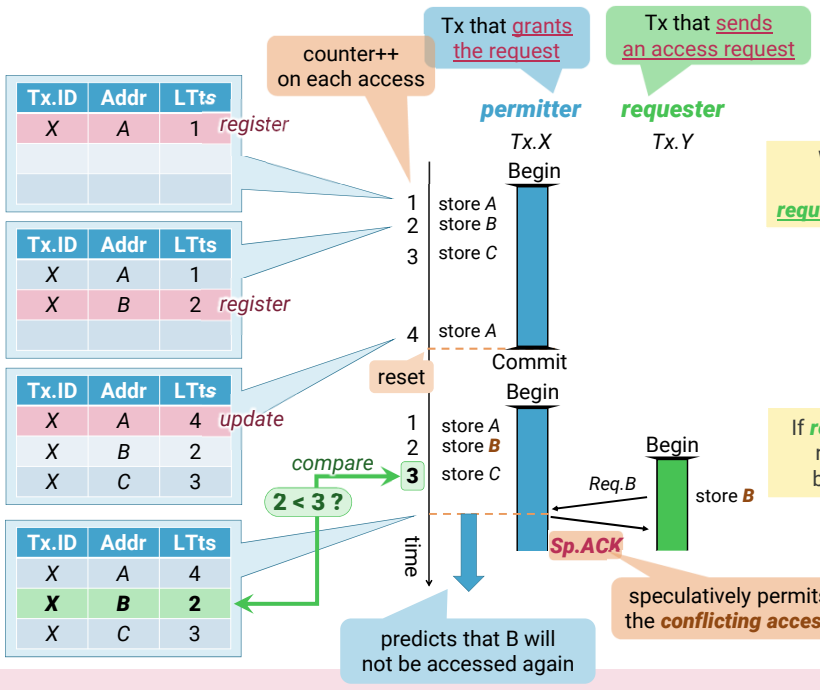
last-touch of "count"

never accessed again until its commit

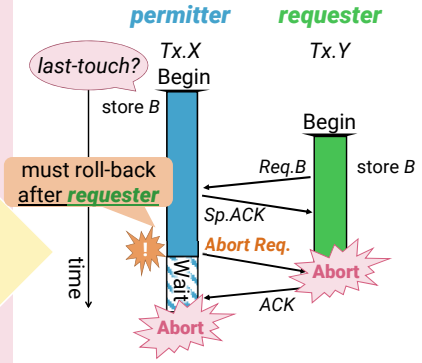
Simplified code of Deque

Granting a Conflicting Access

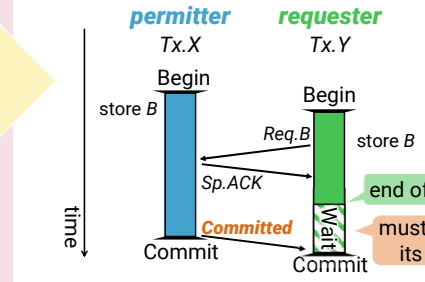
- A counter and a small dedicated table manage ***last-touch*** (*LT*) timestamps.



When ***permitter*** needs to abort, ***requester*** also needs to.

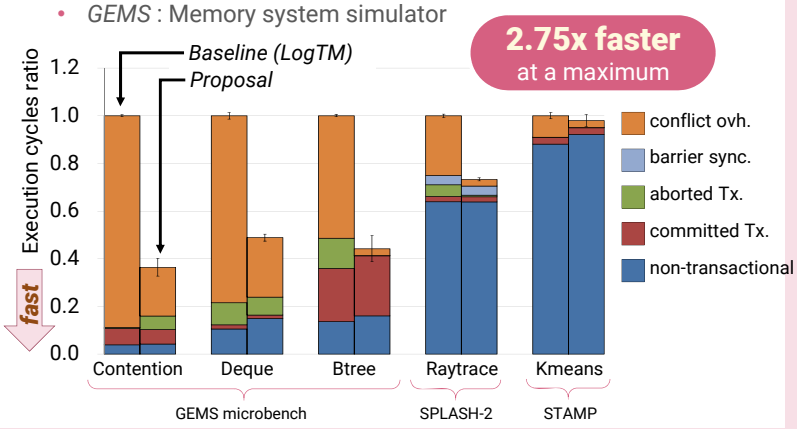


If ***requester*** becomes ready to commit before ***permitter***.



Performance Evaluation

- **Simulation** (16 threads)
  - *LogTM* : Log-based Transactional Memory
    - *Simics* : Full system simulator (SPARC-V9, Solaris10)
    - *GEMS* : Memory system simulator



Hardware Cost

- **Dedicated table**
  - 42bit per one address
  - max # of access destination addresses per Tx: 15,018
- **Each thread manages its *permitter* and *requester***
  16bit + 16bit (16 threads)

Total : 77.1KByte (per one thread) ← can be reduced by managing only limited addresses

Future Work

- Examine the trade-off between storage capacity and performance
- Evaluation with a large variety of programs
- Detailed area cost estimation